REMARKS

In the Non Final Office Action of January 29, 2007, the Examiner: (1) objected to the abstract: (2) rejected claims 1-4, 6-10, 12-16 and 18-26 as allegedly obvious over Eggleston (U.S. Patent No. 6,906,961) in view of Wei (U.S. Patent No. 6,683,817); and (3) rejected claims 5, 11 and 17 as allegedly obvious over Eggleston in view of Kikuchi (U.S. Patent No. 6,594,792);

With this response, Applicant amends claims 1, 6, 8-11 and 14-23. Applicant believes that the pending claims are allowable over the art of record and respectfully request reconsideration.

I. OBJECTIONS TO THE SPECIFICATIONS

In the Office Action, the Examiner objected to the Abstract of the Disclosure for allegedly lacking proper content. To address these concerns, Applicant amends the Abstract to comprise: "A method for streamlining error correction code computation while reading or programming a NAND flash memory. At least some of the illustrative embodiments are methods comprising transferring a data block between a flash memory and a memory controller, and computing an ECC for said data block while transferring the data block." The Abstract is now technically correct and fairly describes various embodiments. It does not refer to purported merits or speculative application of the invention and does not compare the invention to the prior art.

Based on the foregoing, the Applicant respectfully requests that the objection to the Abstract of the Disclosure be withdrawn.

II. ART BASED REJECTIONS

A. Claim 1

Claim 1 stands rejected as allegedly obvious over Eggleston and Wei. Applicant amends claim 1 to remove the "steps of" terminology to ensure a reading that does not invoke Section 112, sixth paragraph, and not to define over any cited art.

Eggleston is directed towards erase block data splitting. (Eggleston Title). In particular, Eggleston teaches flash memory devices that split the user data from the associated overheard data among separate flash memory devices to avoid the issue of potential corruption. (Eggleston Col. 2, lines 60-67). Further, Eggleston teaches a computer system that incorporates flash memory, a processor and a control. (Eggleston Col. 7, lines 36-42).

Wei is directed towards direct memory swapping between NAND flash and SRAM with error correction coding. (Wei Title). In particular, Wei teaches an external memory interface including an error correction coding unit performing block coding of data retrieved from or stored to a NAND flash memory. (Wei Col. 2, lines 20-29). Specifically, Wei teaches an error correction coding unit generating an ECC value after each of the N_D (N_D = 512 bytes) data bytes have been written to or read from the NAND flash memory. (Wei Col. 8, lines 56-64). Hence, Wei appears to teach performing block coding on each page of data to be written.

Claim 1, by contrast, specifically recites "computing an ECC for said data block while transferring the data block." Applicant submits that Eggleston and Wei fail to teach or fairly suggest such a method. In particular, Wei appears to teach an error correction coding unit generating ECC value after a block of has been transferred to or from a NAND flash memory; thus, failing to teach computation of ECC while transferring the data block. Thus, even if the teachings of Eggleston are precisely as the Office Action suggested (which the Applicant does not admit), Eggleston and Wei still fail to teach or fairly suggest "computing an ECC for said data block while transferring the data block."

Based at least on the foregoing Applicant submits that claim 1 is allowable over Eggleston and Wei, and none of the other art of record satisfy the deficiencies of Eggleston and Wei. Accordingly, claim 1 and all claims which depend on claim 1 (claims 2-5) should be allowed.

B. Claim 6

Claim 6 stands rejected as allegedly obvious over Eggleston and Wei. Applicant amends claim 6 to ensure that the claim falls within only one statutory class, and not to define over any cited art.

Claim 6 specifically recites "wherein said controller is configured to shift a data block between the flash memory and the controller while computing an ECC for said data block." Applicant submits that Eggleston and Wei fail to teach or fairly suggest such a method. In particular, Wei appears to teach an error correction coding unit generating ECC value after a block of has been transferred to or from a NAND flash memory; thus, failing to teach computation of ECC while transferring the data block. Thus, even if the teachings of Eggleston are precisely as the Office Action suggest (which the Applicant does not admit), Eggleston and Wei still fail to teach

or fairly suggest "wherein said controller is configured to shift a data block between the flash memory and the controller while computing an ECC for said data block."

Based at least on the foregoing Applicant submits that claim 6 is allowable over Eggleston and Wei, and none of the other art of record satisfy the deficiencies of Eggleston and Wei. Accordingly, claim 6 and all claims which depend on claim 6 (claims 7-11 and 24-26) should be allowed. Applicant amends dependent claims 8-11 to ensure that claims fall within only one statutory class, and not to define over any cited art.

C. Claim 12

Claim 12 stands rejected as allegedly obvious over Eggleston and Wei

Claim 12 specifically recites "a means for shifting the data block between the means for storing and the means for controlling while computing an ECC for said data block." Applicant submits that Eggleston and Wei fail to teach or fairly suggest such a method. In particular, Wei appears to teach an error correction coding unit generating ECC value after a block of has been transferred to or from a NAND flash memory; thus, failing to teach computation of ECC while transferring the data block. Further, even if the teachings of Eggleston are precisely as the Office Action suggest (which the Applicant does not admit), Eggleston and Wei still fail to teach or fairly suggest "a means for shifting the data block between the means for storing and the means for controlling while computing an ECC for said data block."

Based at least on the foregoing Applicant submits that claim 12 is allowable over Eggleston and Wei, and none of the other art of record satisfy the deficiencies of Eggleston and Wei. Accordingly, claim 12 and all claims which depend on claim 12 (claims 13-17) should be allowed. Applicant amends dependent claims 14-17 to ensure that claims fall within only one statutory class, and not to define over any cited art.

D. Claim 18

Claim 18 stands rejected as allegedly obvious over Eggleston and Wei. Applicant amends claim 18 to remove the "adapted to" terminology, and not to define over any cited art.

Claim 18 specifically recites "an ECC engine ~~that computes~~ configured to compute an ECC while transferring a data block between the ECC engine and memory." Applicant submits that Eggleston and Wei fail to teach or fairly suggest such a method. In particular, Wei appears to teach an error correction coding unit generating ECC value after a block of has been transferred to

or from a NAND flash memory; thus, failing to teach computation of ECC while transferring the data block. Further, even if the teachings of Eggleston are precisely as the Office Action suggest (which the Applicant does not admit), Eggleston and Wei still fail to teach or fairly suggest "an ECC engine ~~that computes~~ configured to compute an ECC while transferring a data block between the ECC engine and memory."

Based at least on the foregoing Applicant submits that claim 18 all claims which depend on claim 18 (claims 19-23) should be allowed. Applicant amends dependent claims 19-23 to ensure that claims fall within only one statutory class, and not to define over any cited art.

III. CONCLUSION

In course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and cited art which have yet to be raised, but which may be raised in the future.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. If the Examiner feels that a telephone conference would expedite the resolution of this case, he is respectfully requested to contact the undersigned. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to the Texas Instruments, Inc. Deposit Account No. 20-0668.

Respectfully submitted,

/Utpal D. Shah/

Utpal D. Shah
PTO Reg. No. 60,047
CONLEY ROSE, P.C.
(512) 391-1900 (Phone)
(512) 320-9181 (Fax)
AGENT FOR APPLICANTS